library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity NU is

Port (x: in bit;

y: out bit);

end NU;

architecture arh1 of NU is

begin

process(x)

begin

y <= not(x);

end process;

end arh1;

entity SI is

Port (x, y: in bit;

z: out bit);

end SI;

architecture arh2 of SI is

begin

process(x, y)

begin

z <= x and y;

end process;

end arh2;

entity SAU is

Port (x, y: in bit;

z: out bit);

end SAU;

architecture arh3 of SAU is

begin

process(x, y)

begin

z <= x or y;

end process;

end arh3;

entity SI\_NU is

Port (x, y: in bit;

z: out bit);

end SI\_NU;

architecture arh4 of SI\_NU is

signal a: bit;

begin

process(x, y, a)

begin

a <= x and y;

z <= not(a);

end process;

end arh4;

entity SAU\_NU is

Port (x, y: in bit;

z: out bit);

end SAU\_NU;

architecture arh5 of SAU\_NU is

signal a: bit;

begin

process(x, y, a)

begin

a <= x or y;

z <= not(a);

end process;

end arh5;